I²C Module

Summary

I²C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I²C allows additional devices to be connected to the bus for expansion and system development. The interface operates up to 100 kbps with maximum bus loading and timing. The I²C system is a true multiple-master bus including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.

Features

- Compatibility with I²C bus standard.
- Support for 5-V tolerant devices.
- Multiple-master operation.
- Software-programmable for one of 64 different serial clock frequencies.
- Software-selectable acknowledge bit.
- Interrupt-driven, byte-by-byte data transfer.
- Arbitration-lost interrupt with automatic mode switching from master to slave.
- Transfer completion and read configure interrupt.
- Start and stop signal generation/detection.
- Repeated START signal generation.
- Acknowledge bit generation/detection.
- Bus-busy detection.

Performance and Characteristics

- I²C Gate Number is 2366
- Process：0.18μm (WCS, 1.62V, 120°)

Deliverables

- Verilog HDL source code
- Verilog HDL test pattern
- Documentation

To obtain more information about the I²C *or other C*Core™ products, please contact the C*Core Technology Co., Ltd. by phone: 0512-68091377, email: support@china-core.com or web: http://www.china-core.com.*

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